

# Inventec Corporation

## R&D Division

Board name : Mother Board Schematic

Project : M11D (Santa Rosa)

Version : A02

Initial Date : July 30 , 2007

Approval By : Eric Yang

Check By : Ben Lee

<b>Inventec Corporation</b>	
<small>&lt;Original&gt; Inventec Building,66 Hou-Kang Street Shen-Lin District, Taipei 111, Taiwan TEL:+886-2-2881-0721</small>	
File	
M11D (Merom+Crestline+ICH8M)	
Title	
Rev. 1 of 42	
Date: 2007.07.31.2007	

# Schematic Page Description

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38. 3VS/5VS/1.25VS/1.05VS

39. 1.5VS/1.8V

40. GPU\_Core

41. Audio Board

42. USB Board

43. Glidepad Board

## PCI & IRQ & DMA Description :

IDSEL	CHIP	PCIINT	CHIP	BUSMASTER	REQ	CHIP
None	None	None	None		None	None

## USB & PCI-Express Description :

USB	DEVICE	USB	DEVICE	PCI-E	DEVICE	PCI-E	DEVICE
Port 0	System	Port 5	Docking	Port 1	Express Card	Port 6	None
Port 1	System	Port 6	Express Card	Port 2	LAN		
Port 2	System	Port 7	Card Reader	Port 3	Mini Card(WLAN)		
Port 3	System	Port 8	Web Cam	Port 4	Mini Card(3G)		
Port 4	Mini Card(3G)	Port 9	Bluetooth	Port 5	None		

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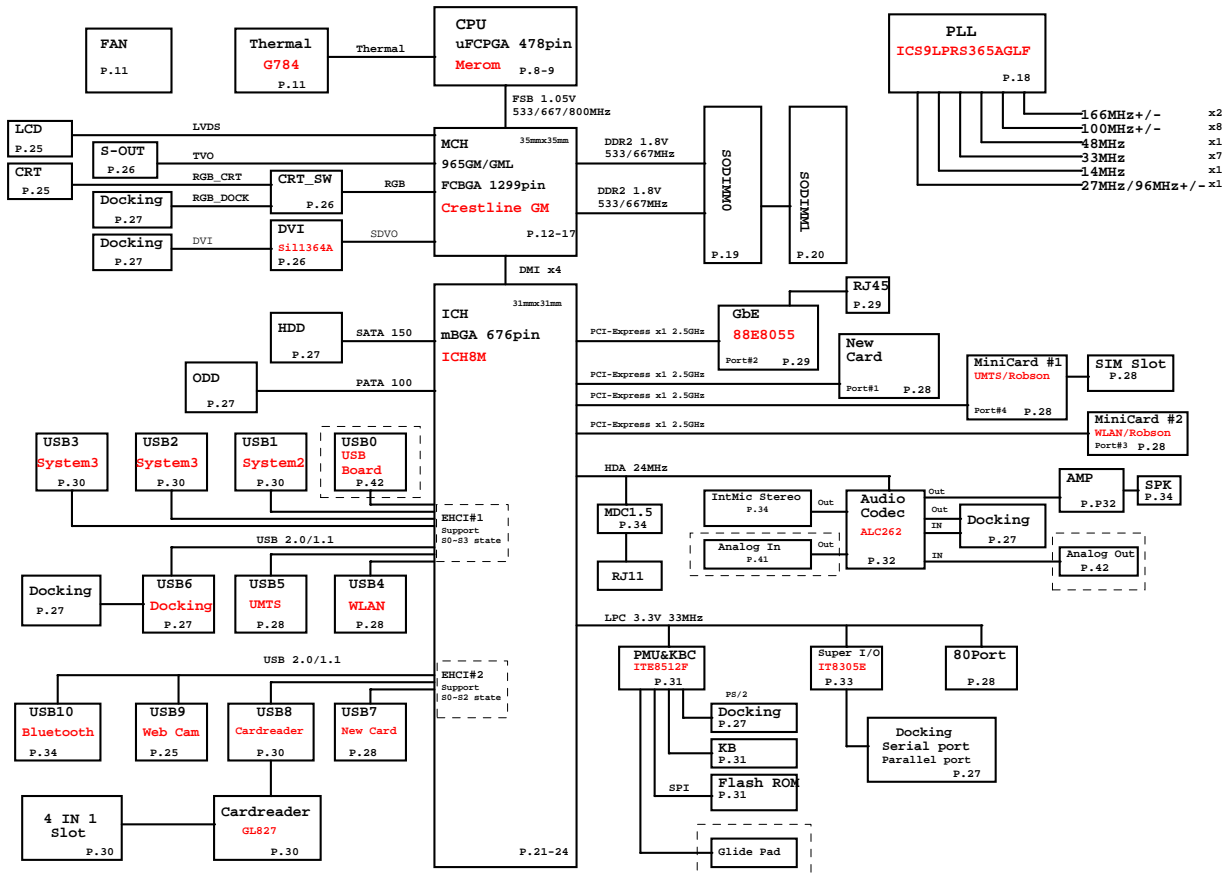
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# System Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH8m by SLP_S3#_3R
+1.8V	1.8V power rail for DDRII by SLP_S5#_3R
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Power Plane
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Merom HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	36A
+1.05VS	Merom: AGTL+ termination 965GM: Core 965GM: AGTL+ termination ICH8m:	0.997V-1.05V-1.102V 1.0V-1.05V-1.1V 0.9475V-1.05V-1.1025V	2.5A 4.6A 1.4A
+1.5VS	Merom PLL 965GM: PCIE 965GM: LVDS 965GM: TVDAC 965GM: Various PLLS analog supply 965GM: DDR DLLS,DDRII,FSB HSIO	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	120mA 1.5A 60mA 24mA 320mA 1.885A
+1.8V	965GM: DDRII System Memory SO-DIMM:	1.7V-1.8V-1.9V	3.1A
0.9VDDT_DDRII	DDRII Terminator:	0.855V-0.9V-0.945V	1.0A
+2.5VS	965GM: PCIE analog 965GM: LVDS analog 965GM: LVDS I/O 965GM: CRT DAC	2.32V-2.5V-2.625V 2.375V-2.5V-2.625V 2.375V-2.5V-2.625V 2.32V-2.5V-2.625V	2mA 10mA 60mA 70mA
+3VS	965GM: HV CMOS 965GM: TVDAC analog ICH8m: ICH8m: ICH8m: ICH8m: ICH8m: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365AGLF Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC: HDD: SATA	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V	40mA 120mA
1.8VS	DVI: SII1364		
+3VA	Thermal Sensor: Lan: Marvell 88E8055B0 Azalia MDC: EC: ITE8512F ICH8m: RTC Flash ROM: BIOS LCD:	3.0V-3.3V-3.6V	1.0A
+5VS	Cardreader: GL827 Azalia Codec: ALC262 FAN: HDD: SATA ODD: PATA Audio AMP: G1432 Woofer AMP: None Inverter:	3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.0A ; R/W: 460mA ; STDBY: 70mA Max: 1.8A ; R/W: 900mA ; STDBY: 45mA
+5VA	USB: x 3 ports	5VA	1.5A
+5VLA	Control Power		

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File

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ANNOTATIONS

Rev: 4 of 40

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# Schematic modify Item and History :

V0.1 First release

V0.1 to AX1

- 1.For FAN PWM Control  
Change C259 From 0.01uF to NU  
Change C538 From 1uF to NU  
Change R118 From 47Kohm to 1Kohm  
Change R119 From 4.7Kohm to 0 ohm  
Change R415 From 10 ohm to NU
- 2.For Power sequence issue (VRMPWRGD From CORECLK\_EN Change to VCORE\_GD)  
Change R131 From NU to 0 ohm  
Change R133 From 100K ohm to NU  
Change U13 From TC7SZ04FU to NU
- 3.For Power sequence issue (Delay VCORE\_GD to PM\_ICH\_PWROK )  
ADD C1202 to 0.1uF  
ADD R1116 to 100K ohm  
ADD D34 BAT54C-7
- 4.For VESA Specification Requirement (MB Side)  
Change C5,C6,C8 From 22pF to 18pF  
Change L3,L4,L5 From 17ohm 600mA to 10ohm 500mA  
Change C9,C10,C11 From 10pF to NU  
Change R4,R5,R6 From 200ohm to 220ohm
- 5.For VESA Specification Requirement (Docking Side)  
Change R266,R267,R268 From 200ohm to 220ohm
- 6.For Serial RING Wake (Change from to EC)  
Change RING# single connect to U9 IT8512E Pin119  
Change U4 MAX3243 Pin26 From 3VS to 3VA
- 7.For Audio  
Change Speaker single change connect to pin35,36  
Change Hearphone single change connect to pin39,41  
Change R586 From 5.1Kohm to 39.2Kohm  
DEL R584,R580,R588,R589,C679,U46
- 8.For EMI Requirement  
ADD C1206-C1251 0.1uF in 3VA,5VA,DCIN,VADPTR\_DOCK  
ADD C1204,C1205 1000pF in SW Board connecter  
ADD L1105-L1108 in Speaker connecter  
Change Q29,Q30,Q32,Q33 From FDS6676AS to FDMS8670S  
ADD C1252-C1254 0.1uF in USB\_VCC1
- 9.For SATA Eye issue  
Change C587,C591 From 3300pF to 3900pF
- 10.For Docking DVI  
  
TX2 Change to CN28 Pin 13,14  
TX1 Change to CN28 Pin 16,17  
TX0 Change to CN28 Pin 19,20  
TXC Change to CN28 Pin 22,23

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Rev

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Schematic Modify

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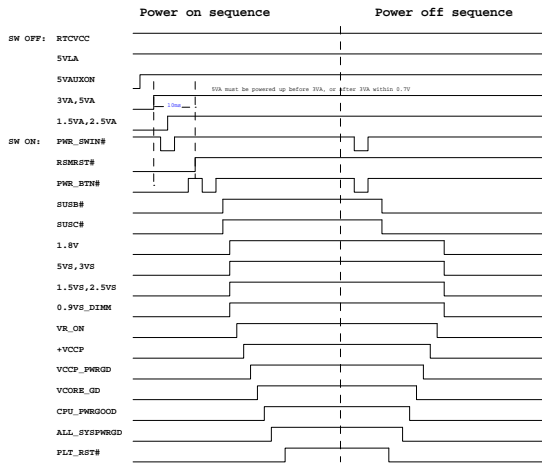
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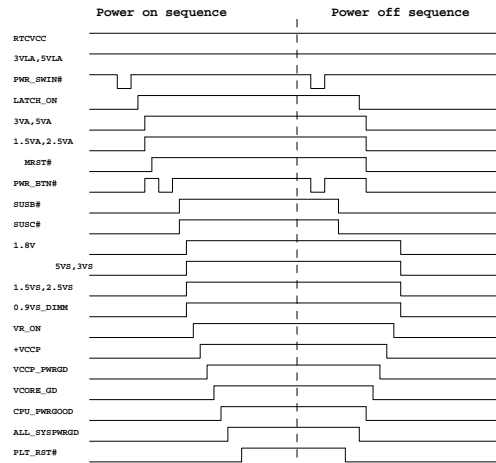
48

# SYSTEM POWER ON/OFF SEQUENCE

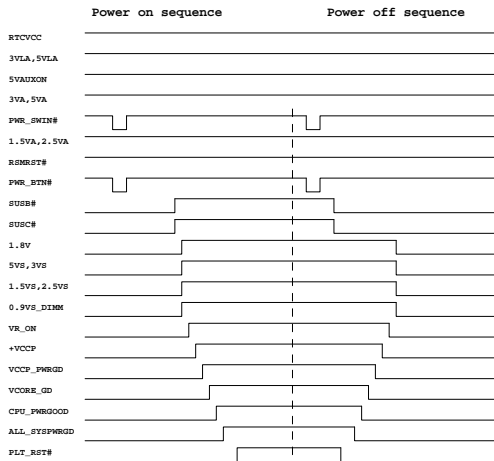
Power on/off sequence AC insert(First)



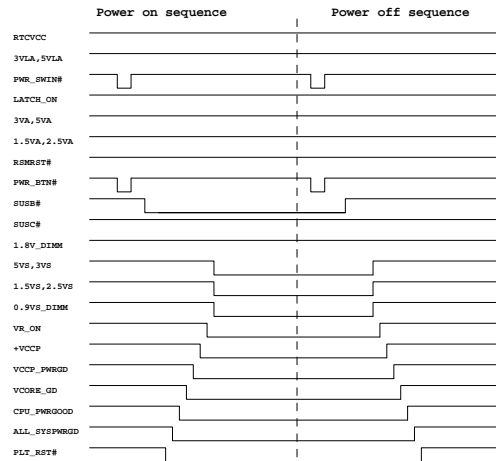
Battery only Power on/off sequence



Power on/off sequence AC insert(S4)



Suspend resume sequence(S3)



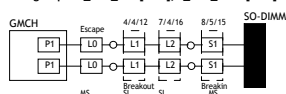
## DDRII Layout Guideline :

## Crestline DDRII Layout Guidelines

## DDRII Signal Groups

Group		Length Matching and Length Formulas		
Data	M_A_DQ[0:15]/M_B_DQ[0:15] M_A_DQ[16:31]/M_B_DQ[16:31] M_A_DQ[32:47]/M_B_DQ[32:47] M_A_DQ[48:63]/M_B_DQ[48:63]	Signal Group	Minimum Length	Maximum Length
Address	M_A_A[13:31]/M_B_A[13:31] M_A_A[32:47]/M_B_A[32:47] M_A_CAS[0:15]/M_B_CAS[0:15] M_A_CAS[16:31]/M_B_CAS[16:31]	Control-to-Clock	Clock - 1.0°	Clock - 0.0°
		Command-to-Clock	Clock - 1.0°	Clock - 1.0°
		Strobe-to-Clock	Clock - 0.5°	Clock - 1.0°
		Data-to-Strobe	Strobe - 220mils	Strobe - 180mils
Control	M_CS[0:15] M_CS[16:31] M_ODT[13:31]			
Clock	M_CLK_DQ[0:15] M_CLK_DQ[16:31]			
Feedback	SA_RC[VEN]/SB_RC[VEN]			

CLK group : M\_CLK\_DDR[3..0],M\_CLK\_DDR#[3..0]

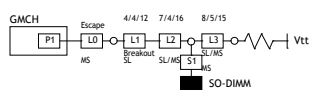


Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Minimum Serpentine Spacing	Inner Layer: 12 mils Outer Layer: 15 mils
Package Length Range- P1	350 mils - 625 mils
Min. Serpentine Spacing	23 mils
Trace Length Limit - L0 (MS)	Nominal Trace Width: 5 mils, 4 mils Length Limit: Max = 50 mils (Excape) Min. Trace Spacing: 5 mils, 4 mils
Trace Length Limit - L1 (SL) (Breakout length segment)	Length Limit: Max = 700 mils Nominal Trace Width: 4 mils Trace Spacing (pair): 4 mils Min. Trace Spacing (Other): 12 mils
Stab Length S1 Stab from via to SO-DIMM	Max = 200 mils (Breakout)
MS Length Limits - L0 = L1 = L2 = S1	Min = 500 mils Max = 6000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 6500 mils
Maximum Via Count	2 (Per side)
CK to CK# Length Matching	Total pair length to within 5 mils
Click to Click Length Matching (Total Length)	Inner Layer: a close to +/- 0.5 mils Trace Channel a close to +/- 0.5 mils
Breakout Exceptions (Reduce geometries for GNC# Break-out region)	Inner Layer: +/- 6 mils to only other D062 Outer Layer: +/- 15 mils to other D062 Max. breakout length is 500 mils
Breakout Exceptions (Reduce geometries for SO-DIMM Break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other D062 Max. breakin length is 200 mils

Feedback group :  
SA\_RCVENIN[,SA\_RCVENOUT[,SB\_RCVENIN[,SB\_RCVENOUT[

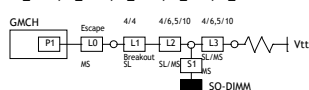
These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

Control group : SM\_CKE[3..0],SM\_CS#[3..0],SM\_ODT[3..0]



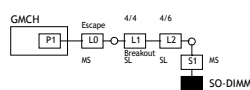
Topology	Point-to-point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 $\pm$ 15 $\Omega$
Nominal Trace Width	Inner Layer: 4 mils Outer Layer: 3 mils
Minimum CTRL Trace Spacing	Inner Layer: 8 mils Outer Layer: 10 mils
Minimum Spacing to Other D0R2	Inner Layer: 12 mils Outer Layer: 15 mils
Minimum Isolation Spacing to non-D0R2	25 mils
Package Length P1	750 mils $\pm$ 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length L1-Stub from via to D0MM	Max = 200 mils (Breakout)
Trace Length Limits - L1 + L2 + L3	Max = 500 mils
From GMIH back to 200MHz pad	Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + L3	Max = 5000 mils
From GMIH die to D0MM pad	Max = 1500 mils
Parallel Termination Resistor	56 $\pm$ 5 $\Omega$
Maximum Via Count	3
CTRL to SCAS/GMIH Length Matching	(CLK-L0) $\pm$ CTRL $\pm$ (CLK-L0)
Package Length including package	
Breakout Exceptions (Relax the geometries for GMIH back-end region)	Inner Layer: 4 mils spacing allowed Outer Layer: 5 mils spacing allowed Minimum stub length is 300 mils

Command group :  
SA\_MA[13..0],SB\_MA[13..0],SA\_BS[2..0],SB\_BS[2..0],SA\_RAS#,  
SB\_RAS#,SA\_CAS#,SB\_CAS#,SA\_WE#,SB\_WE#



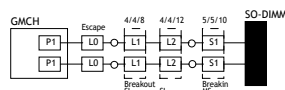
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	53 $\pm$ 15 $\Omega$
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum GND Bus Trace Spacing	Inner Layer : 4 mils Outer Layer : 10 mils
Minimum Spacing to Other D0R2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-D0R2	25 mils
Package Length P1	750 mils $\pm$ 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO DIMM	Max = 200 mils (Breakout)
MS Length L2s - L0 + L1 + L2 + S1 - From GNDx ball to SO DIMM pad	Min = 500 mils Max = 500 mils
Total Length P1 + L0 + L1 + L2 + S1 - From GNDx die to SO DIMM pad	Min = 500 mils Max = 1500 mils
Trace Length Limit - L2	Max = 1500 mils
Parallel Termination Resistor	56 $\pm$ 5 $\Omega$
Maximum Via Count	3
CTRL to SOx/S0x Length Matching (Total Length including package) Reference Exceptions: Reduce geometries for GNDx break-out region)	(CLK1_0) $\pm$ GND $\pm$ (CLK1_0) Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed

Data group : SA\_DQ[63..0],SB\_DQ[63..0],SA\_DM[7..0],SB\_DM[7..0]

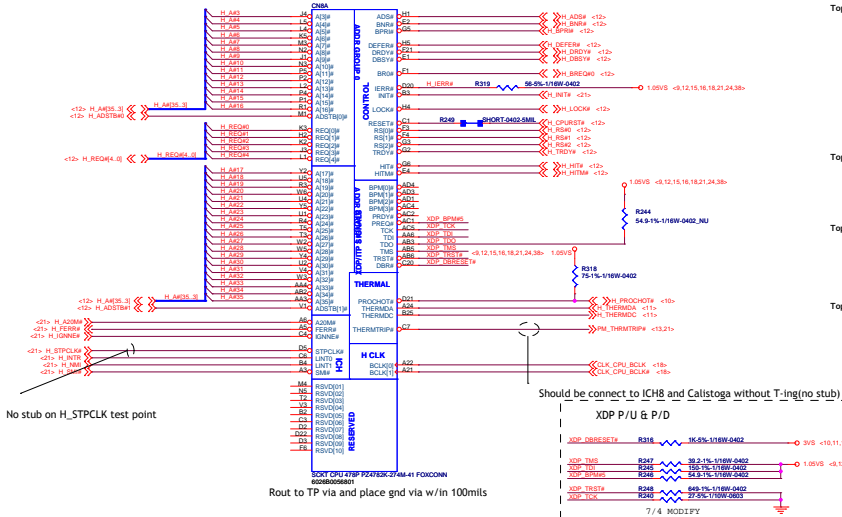


Topology	Point-to-point
Reference Plane	Ground
Characteristic Trace Impedance	55 $\pm$ 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing for Other D0R2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-D0R2	25 mils
Trace Length Pin 1	750 mils $\pm$ 350 mils
Trace Length Limit - L0	Max = 500 mils (Breakout)
Trace Length Limit - L1	Max = 500 mils (Exception)
Stub Length S1-Stub from via to SQ-DMM	Max = 200 mils (breakout)
Trace Length Limits - L0 + L1 + L2 + S1	Inner Layer : 4 mils Outer Layer : 5 mils
From GNCB lead to SQ-DMM pad	Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GNCB lead to SQ-DMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximum Via Count	2
DQ/DM to DQS Length Matching	Match
Total Length Difference	2 $\pm$ 20mil, per byte lane
Backdriven Exceptions (Reduce geometries for GNCB break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Minimum length is 500 mils

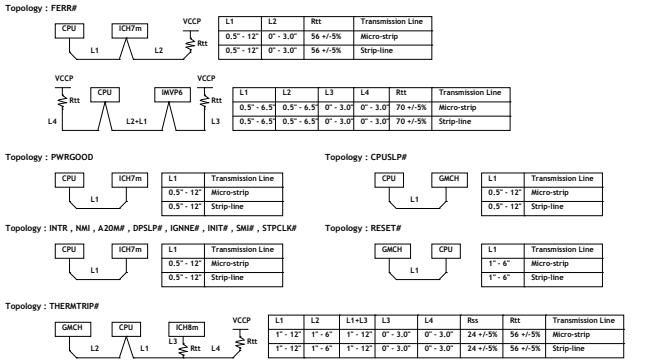
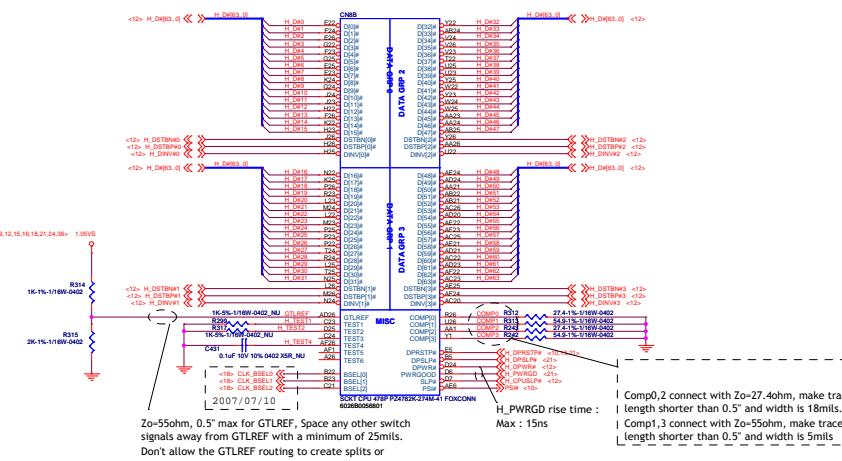
Data Strobe group : SA\_DQS[7..0],SA\_DQS[7..0]#,SB\_DQS[7..0],SB\_DQS[7..0]#



	3A	3B
Topology		Differential Pair Point-to-Point
Reference Plane		Ground
Single Ended Trace Impedance		55 + / - 10%
Differential Mode Impedance		85 + / - 10%
Normal Trace Width		Inner Layer : 4 mils Outer Layer : 5 mils
Normal Trace to DQ5 Spacing (edge to edge)		Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ5 to DQ Spacing		Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing		Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to other DOR2		Inner Layer : 12 mils Outer Layer : 17 mils
Minimum Isolation Spacing to non-DOR2		25 mils
Package Length Range - P1		750 mils + / - 350 mils
Trace Length Limit - L1		Max = 500 mils (Escape)
Trace Length Limit - L2		Max = 500 mils (breakout)
Stitch Length 51-Stitch from via to SO-DIMM		Max = 200 mils (breakout)
HL Length Limits - L10 + L12 + S11		Min = 500 mils
From GNC1 ball to SO-DIMM pad		Max = 4500 mils
Total Length - P1 + L10 + L12 + S11		Max = 5000 mils
From GNC1 die to SO-DIMM pad		
Maximum Via Count		2 (Per side)
DQ5 to DQ5F Length Matching		Match total length to within 5 mils
Click to Clock Length Matching		$(CLK-0.5) > (DQ5-DQ5F) > (CLK1-0.7)$
Breakout Escapes (Reduce geometries for GNC1 based board region)		Inner Layer : 8 mils to other DOR2 Outer Layer : 10 mils to other DOR2 Max. breakout length is 500 mils
Breakout Escapes (Reduce geometries to SO-DIMM break-in region)		DQ5 to DQ5F spacing rule waived at connector spacing of 10 mils to other DOR2 Max. break length is 200 mils



AR[32:39], APM[0:1]: Leave escape routing on for future functionality



**FSB Common Clock Signal Layout Guide:**

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
H_ADSP#, H_BNRP#, H_BPRF#, H_BROF#, H_DBSYF#, H_DEFERF#, H_DPWR#, H_DRDYF#, H_HITF#, H_HITM#, H_LOCKF#, H_RS[2..0], H_TRDYF#, H_CPURSTF#	Strip-line (Int. Layer)	1.0 - 6.5 inch	55 +/- 15%	W=4 & S=8 mils
	Micro-strip (Ext. Layer)	1.0 - 6.5 inch	55 +/- 15%	W=5 & S=10 mils

**FSB Source Synchronous Data Length Variation and Strobe Matching Requirements:**

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
H_DINVP[3..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_DATA[63..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_DSTBNP[3..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_DSTBP[3..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils

**FSB Source Synchronous Address Length Variation and Strobe Matching Requirements:**

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
H_A[15..3]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_REQ[4..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_ADSTB[1..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=12 mils

**FSB Source Synchronous Address Signal Routing:**

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
H_A[15..3]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_REQ[4..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_ADSTB[1..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=12 mils

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**M11D (Merom+Crystalline+ICH8M)**

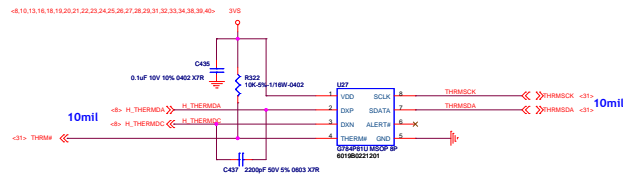
Merom Processor(1/2)



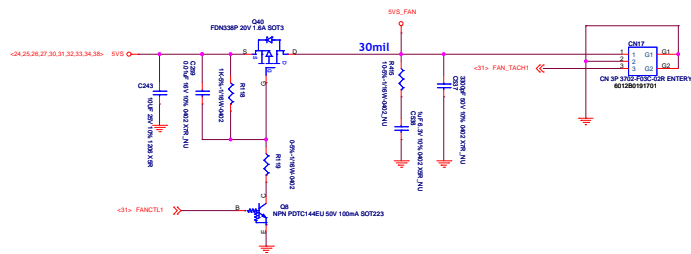




## THERMAL SENSOR



## Fan control



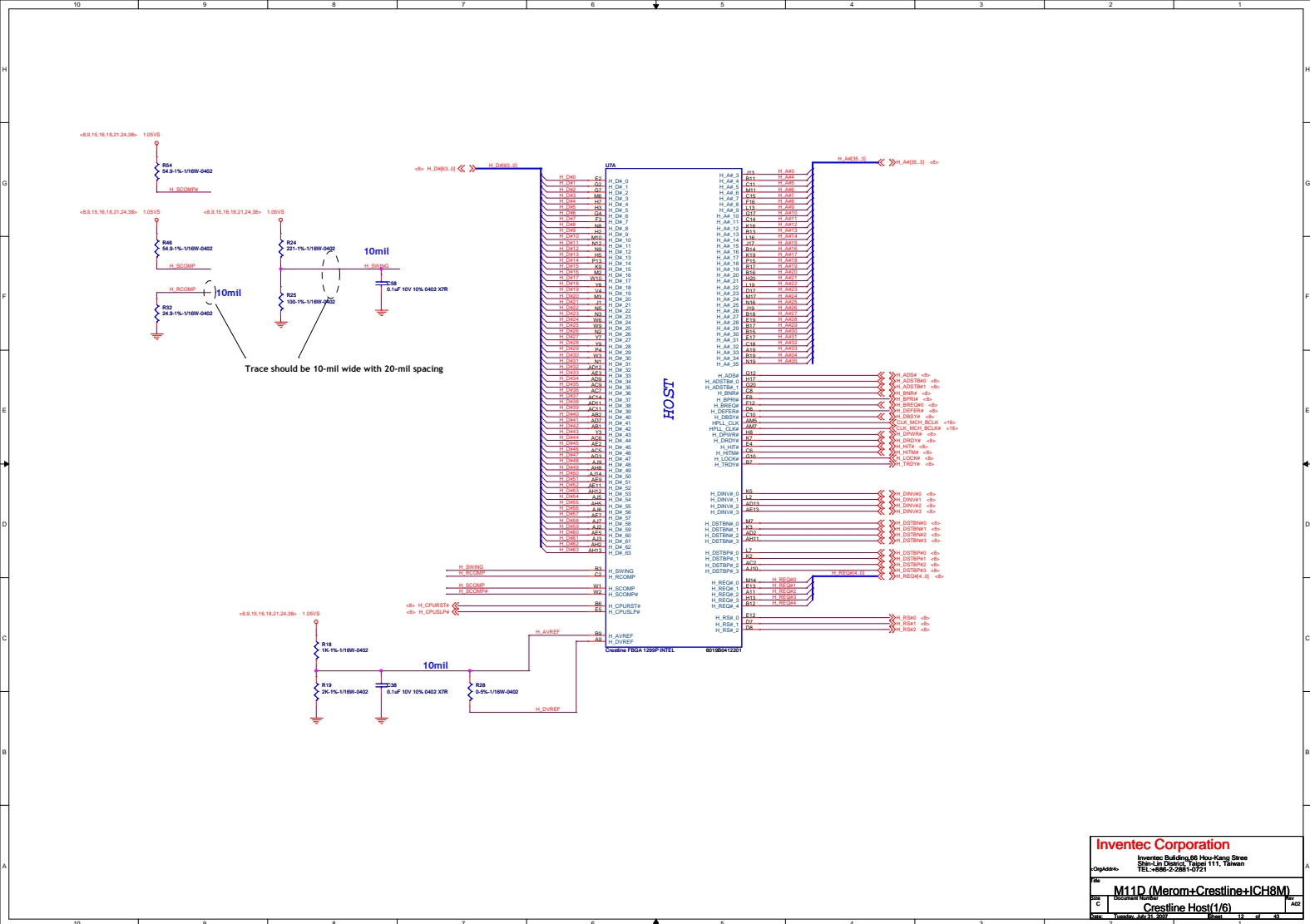
Inventec Corporation

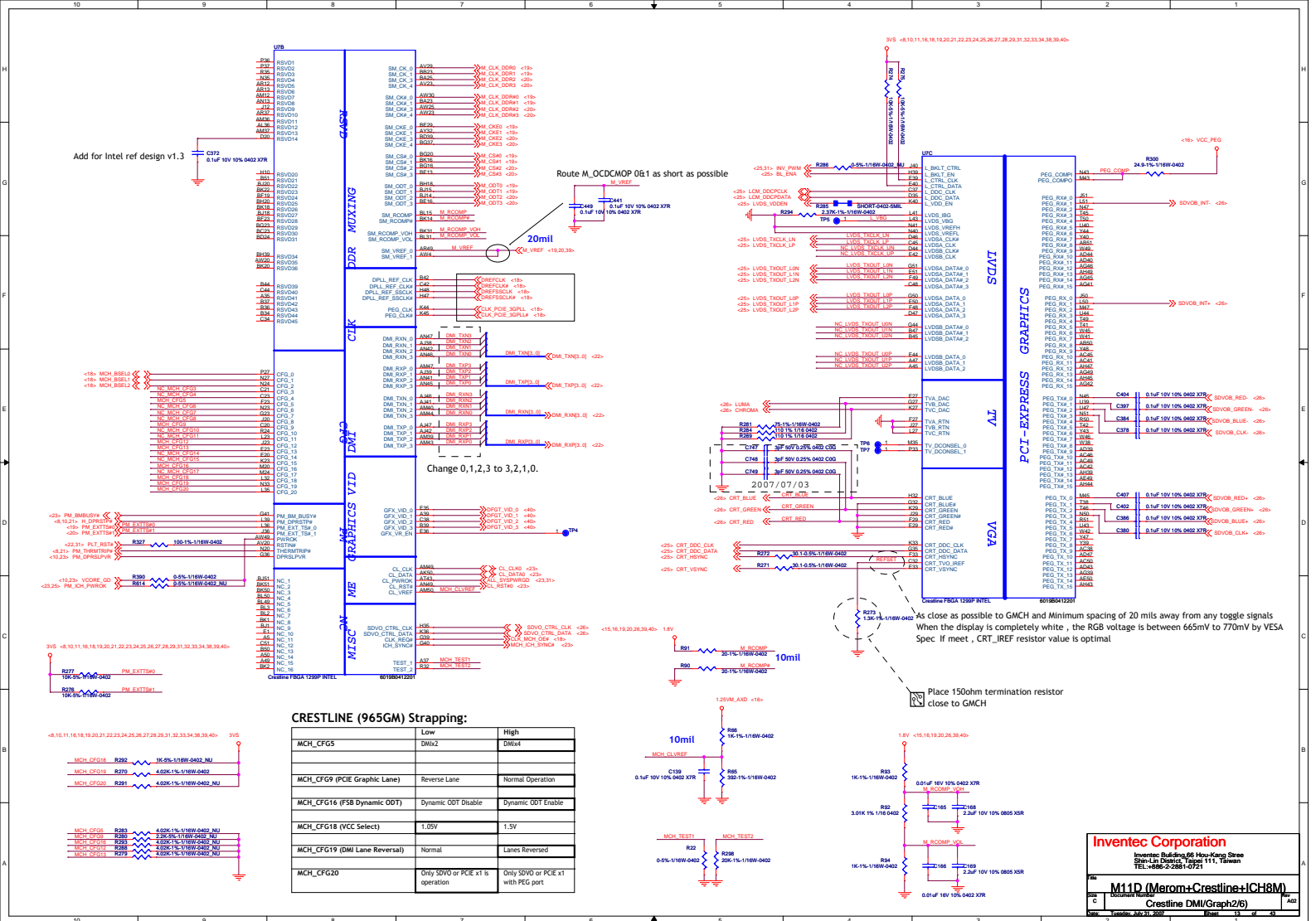
Inventec Building, 66 Hou-Kang Street  
Shin-Lin District, Taipei 111, Taiwan  
TEL: +886-2-2881-0721

**M11D (Merom+Crestline+ICH8M)**

Size C	Document Number <b>CPU Thermal</b>
Date: Tuesday, July 31, 2007	Sheet

Date: Tuesday, July 31, 2007 Sheet 11 of 43

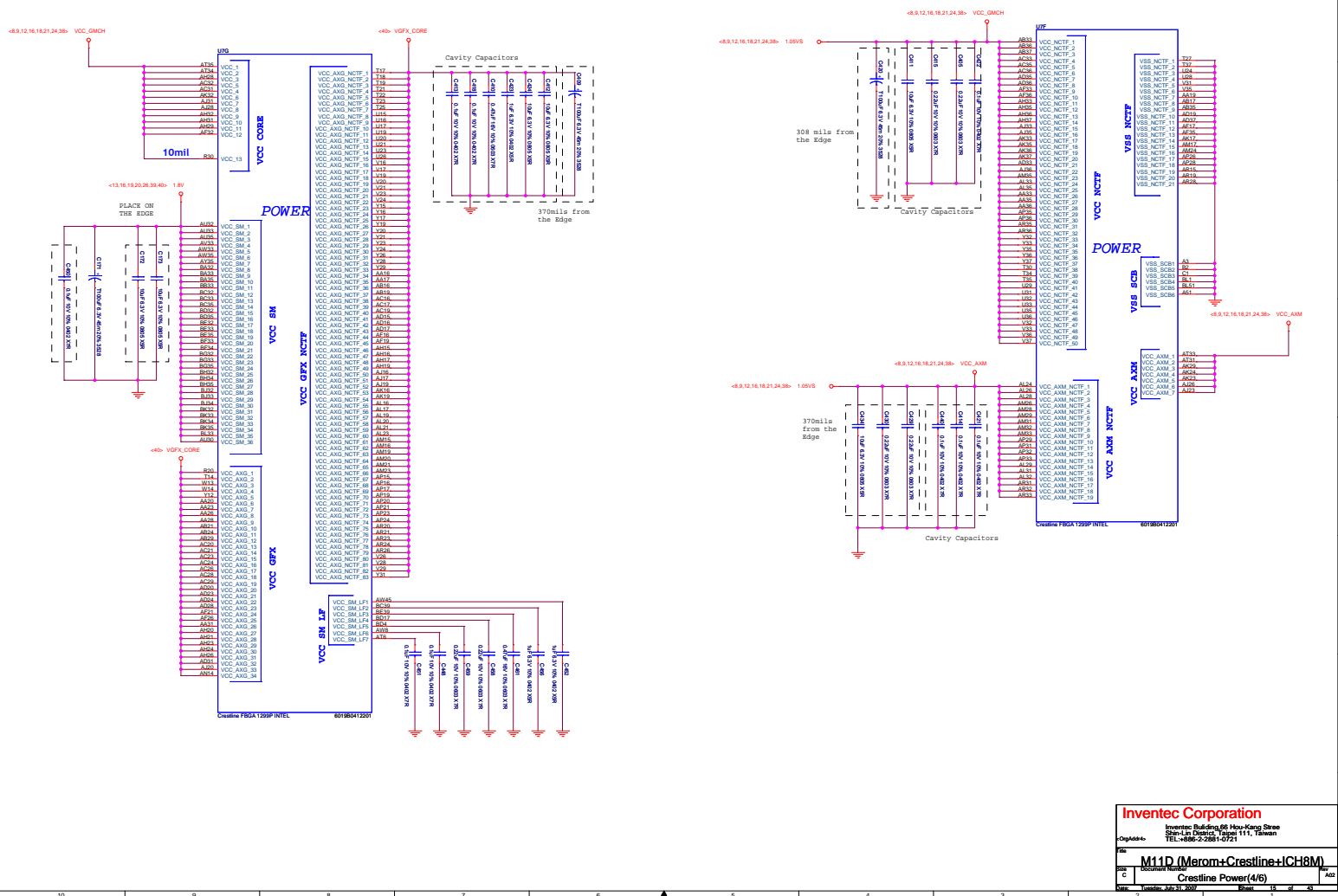


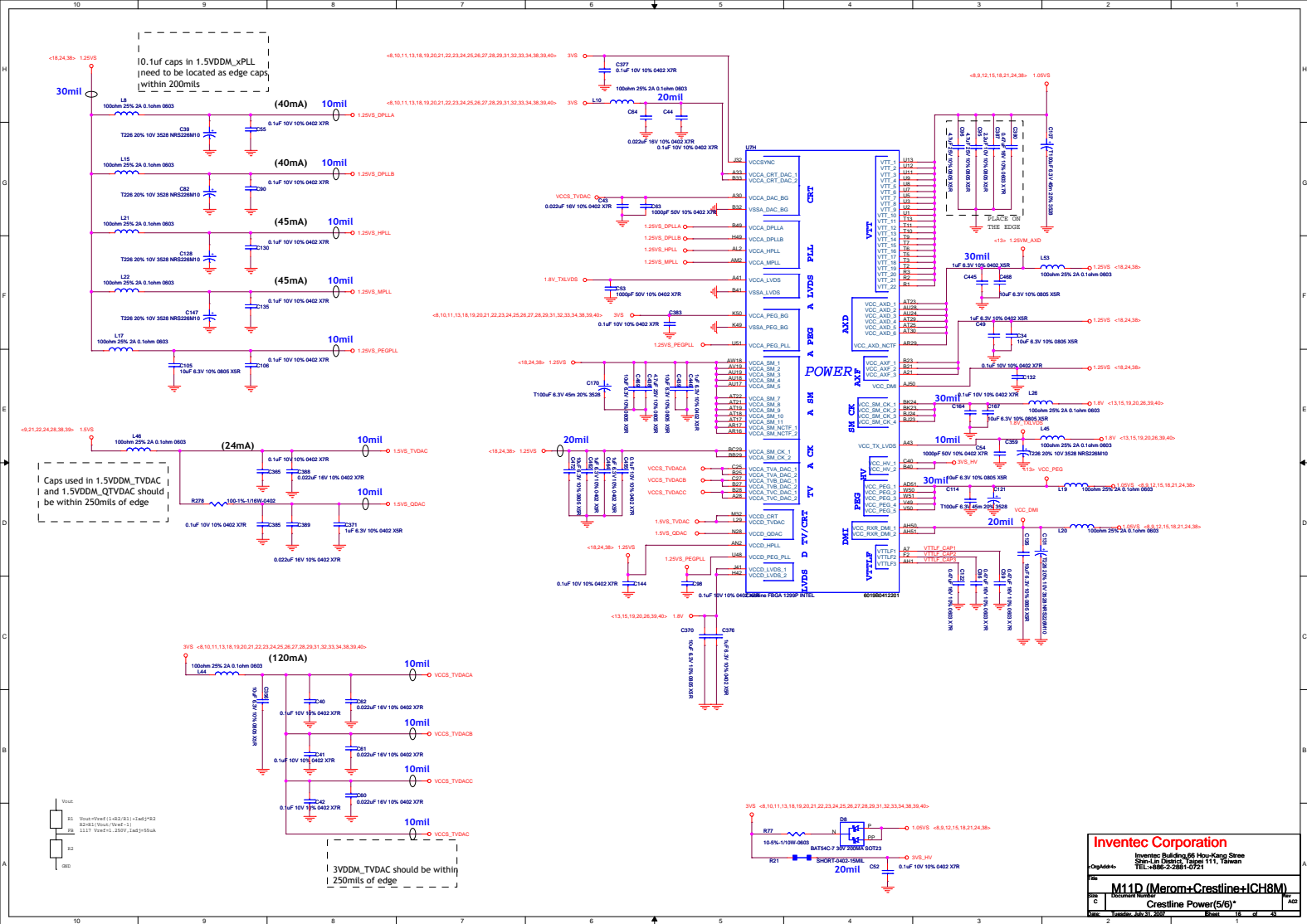


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M11D (Merom+Crestline+ICH8M)  
Crestline DMU/Graph2/6  
Rev: 1.0  
Date: 2007.07.20

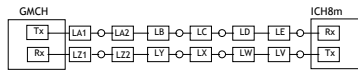
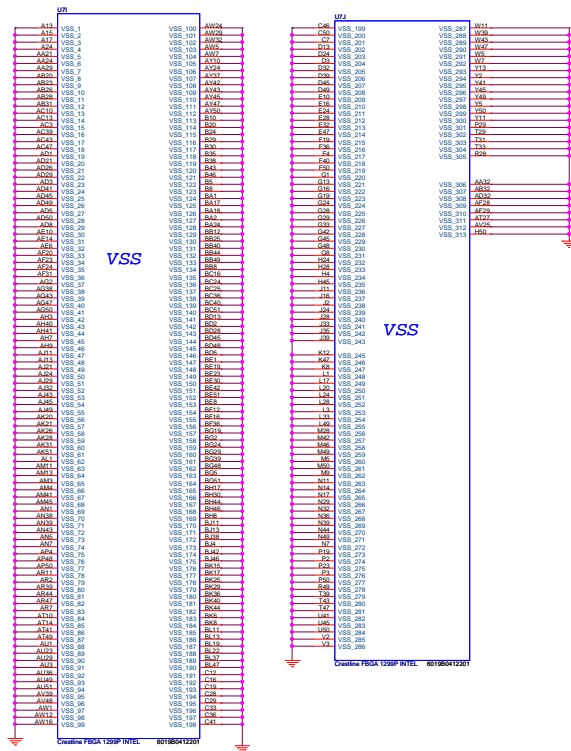








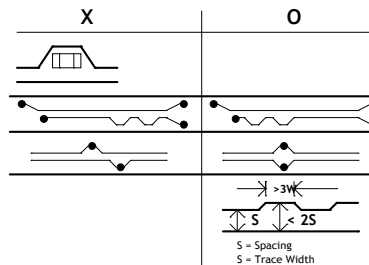
## DMI Routing Guideline



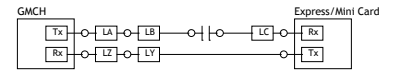
Breakout in LA/LZ	Main Route LA/LZ		Breakout in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Road Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer: 4 mils Outer Layer: 5 mils	Inner Layer: 4 mils Outer Layer: 5 mils
Nominal Discontinuous-Pair Pitch	Inner Layer: 7 mils Outer Layer: 7 mils	Inner Layer: 4 mils Outer Layer: 5 mils
Pair-to-Pair Pitch	Inner Layer: 12 mils Outer Layer: 9 mils	Inner Layer: 12 mils Outer Layer: 9 mils
Bo-to-Bo Pitch	Inner Layer: 12 mils Outer Layer: 20 mils	Inner Layer: 15 mils Outer Layer: 12 mils
Reference Plane	Ground	Ground
Spits/Voids	No routing over plane spits No routing over voids	
Trace Length-L1 (GMCH Breakout)	Max = 2500 mils	
Trace Length-L8 (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-L2 (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-C1 (LA-L8-CC-D1-E3)	Max = 8000 mils	
Trace Length-V1 (ICH7m Breakout)	Max = 400 mils	
Trace Length-V2 (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-L2 (Via2 to Via3)	Max = 5900 mils	
Trace Length-L3 (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-L2 (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-L2 (LV-LW-LX-LY-L2)	Max = 400 mils	
Trace Length-L2 (LV-LW-LX-LY-L2)	Max = 8000 mils	

\*\*\* Match the trace lengths of the complementary signals within each differential pair to  $\pm 5$  mil

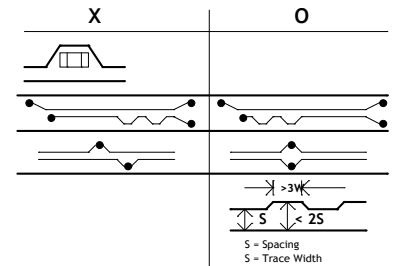


## PCIE Routing Guideline



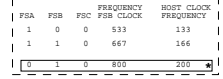
Pinback/In LE/LV	Main Route LE/LV	Main Route LE/LV	Pinback/In LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip
Parameter		Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance		55 +/- 15%	55 +/- 15%
Nominal Trace Width		Inner Layer : 4 mils Outer Layer : 5 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal Differential Trace Space		Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch		Inner Layer : 32 mils Outer Layer : 39 mils	Inner Layer : 27 mils Outer Layer : 32 mils
Bus-to-Bus Pitch		Inner Layer : 32 mils Outer Layer : 20 mils	Inner Layer : 18 mils Outer Layer : 12 mils
Reference Plane		Ground	Ground
Splices/Voids		No routing over plane splits No routing over voids	
Trace Length-LA (IC/HM Breakout)		Max = 400 mils	
Trace Length-LB (IC/HM Breakout to AC cap)		Max = 10750 mils	
Trace Length-L2 (AC cap to PCIE CH)		Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)		Max = 12000 mils	
Trace Length-LY (PCIE CH to IC/HM Breakout)		Max = 11950 mils	
Trace Length-L2 (IC/HM Breakout to AC cap)		Max = 400 mils	
Trace Length-L2 (LY+LZ)		Max = 12000 mils	

\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



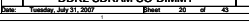
The diagram shows four digital signals over time. The signals are CLK\_BSEL0, FSA, FSB, and FSC. CLK\_BSEL0 is a clock signal that transitions from low to high. FSA, FSB, and FSC are data signals that are sampled by CLK\_BSEL0. FSA is sampled at the first rising edge of CLK\_BSEL0, FSB at the second, and FSC at the third. The signals are labeled with their respective values: FSA = 0, FSB = 1, and FSC = 0.

2007/07/24



## DIMM 1

## DIMM 2



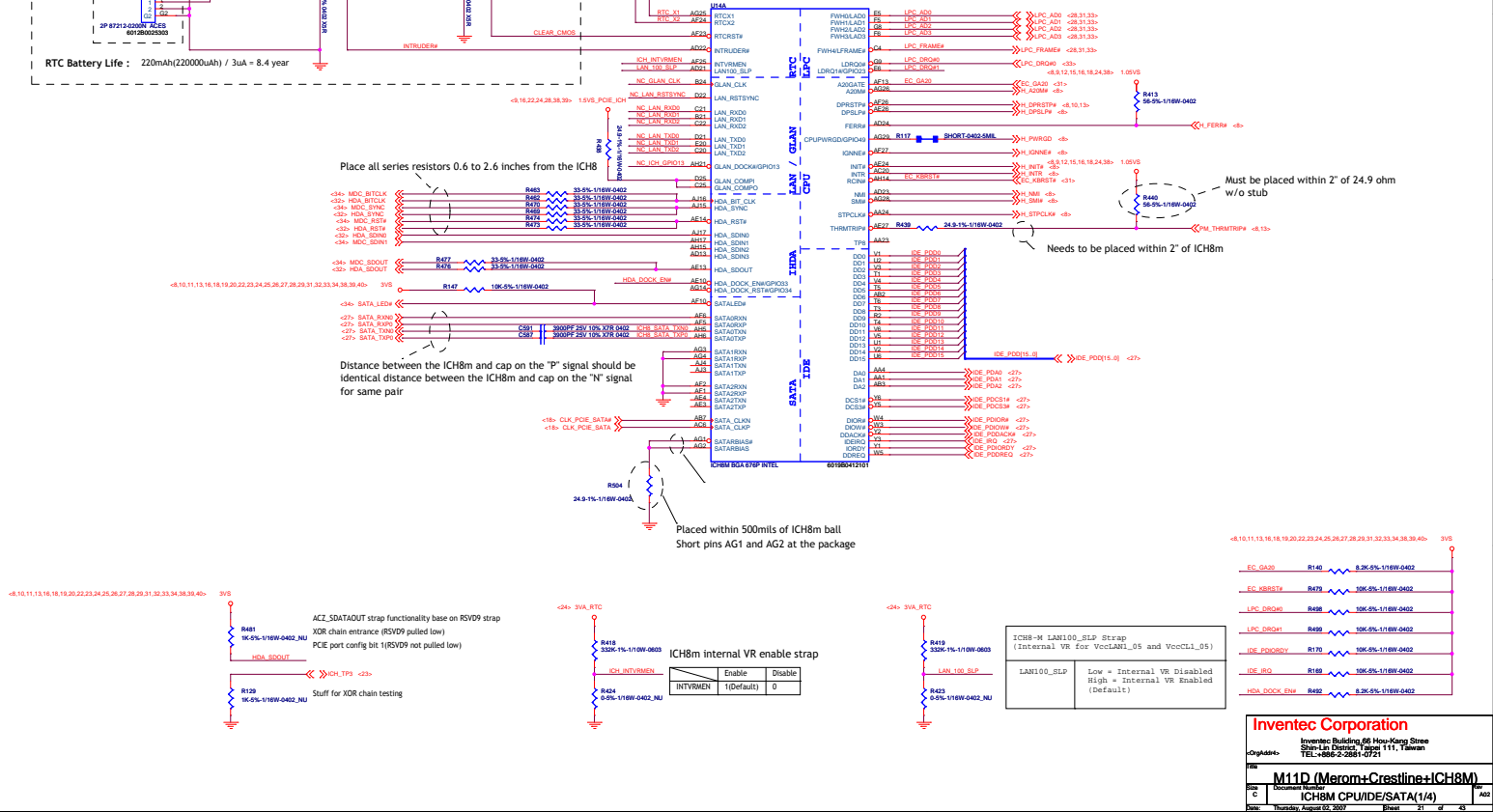
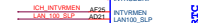
20mil

- $$0\mu\text{Ah}) / 3\mu\text{A} = 8.4 \text{ year}$$

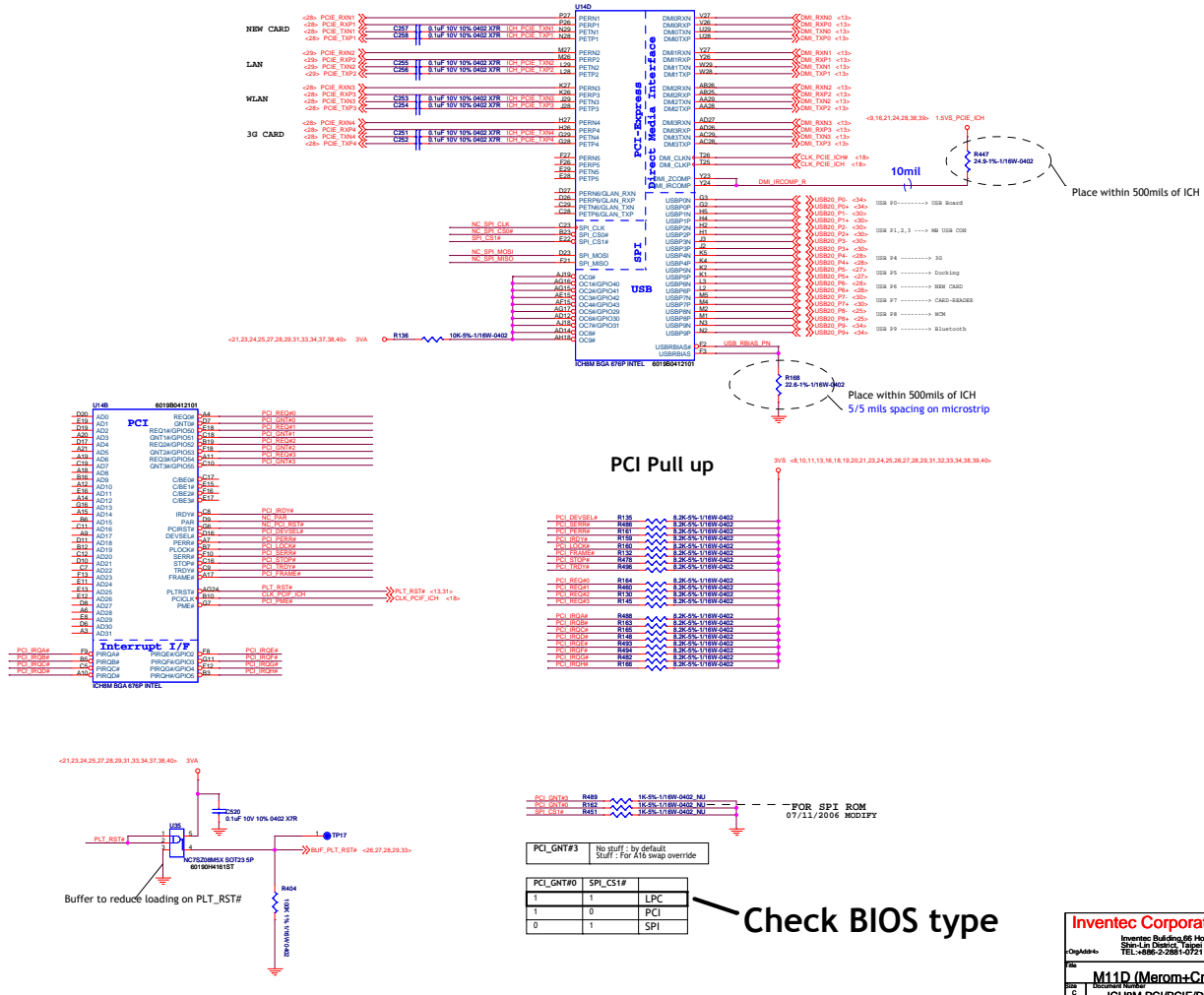


10mil

- ETC



PCIE AC coupling caps need to be within 250mils of the driver



PCI\_GNT#3 No stuff; by default  
Stuff: For A16 swap override

PCI_GNT#0	SPI_CS#
1	1
1	0
0	1

Check BIOS type

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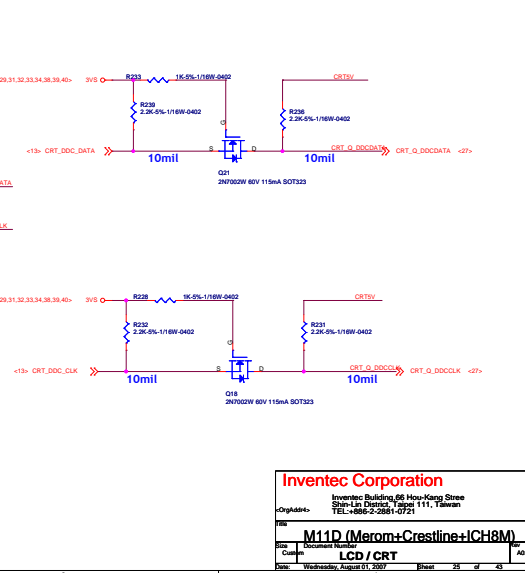
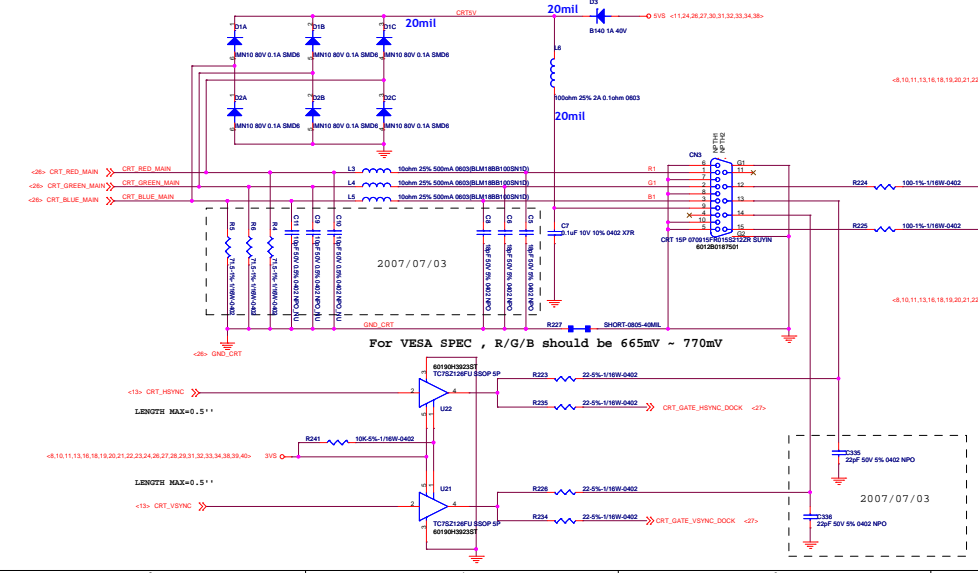
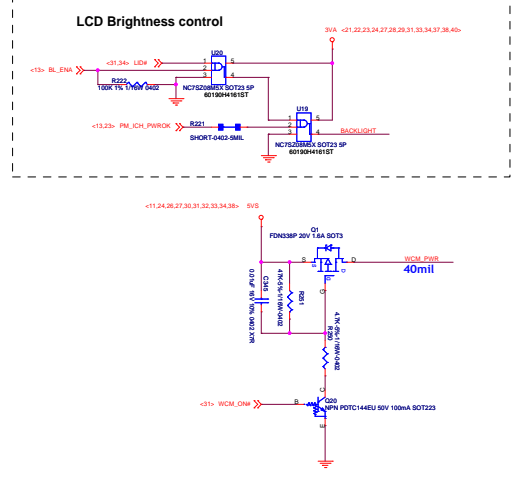
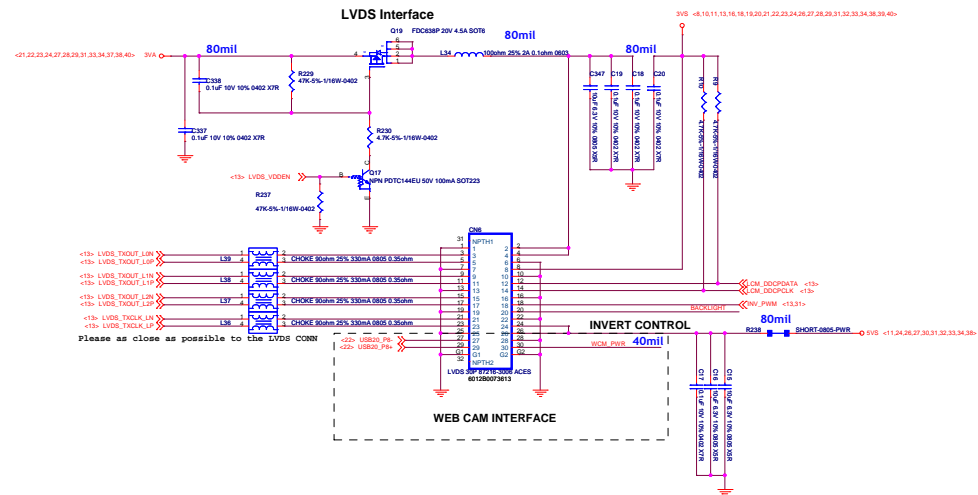
**M11D (Merom+Crestline+ICH8M)**  
IC#8M PCI/PCIe/DMI/USB(24)

Model: M11D Date: 07/21/2007









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**M11D (Merom+Coreline+ICH8M)**

**LCD / CRT**

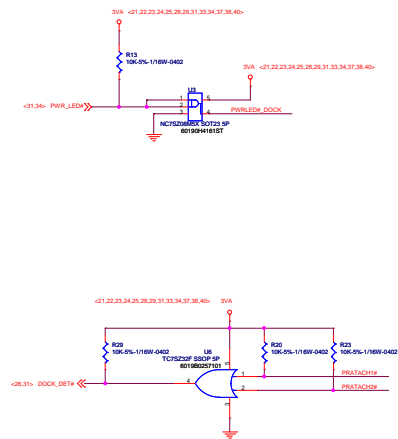
Rev: 1.0 Date: 01/2007 Page: 25 of 45



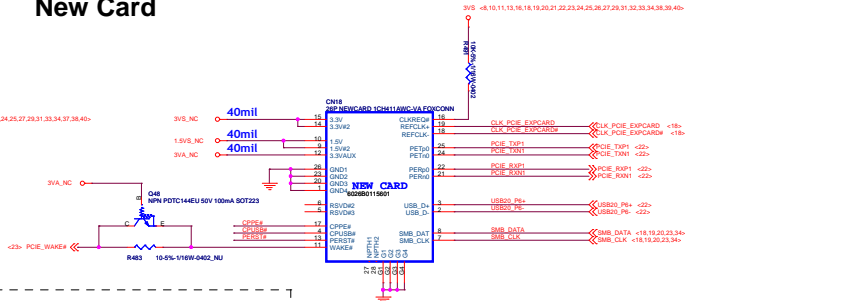
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2007/07/03

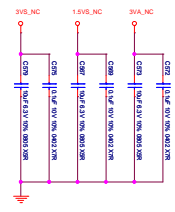
DOCKING TOP BCT110505 V1.6a  
601280156501



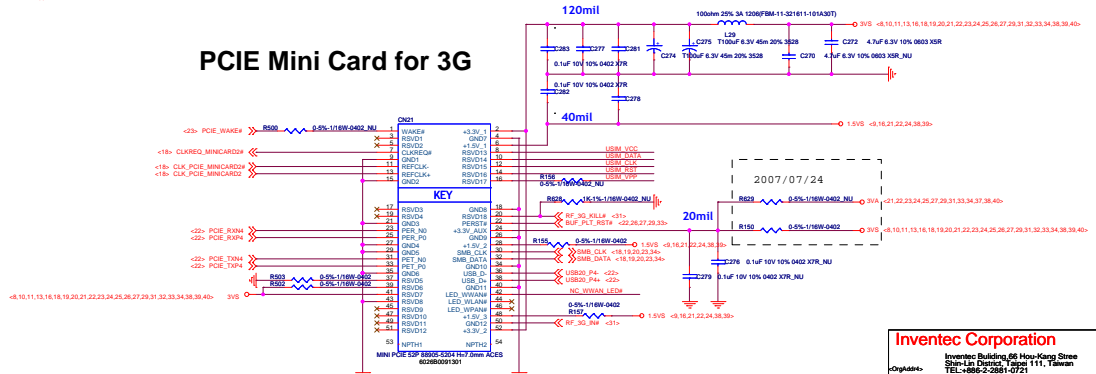
## New Card



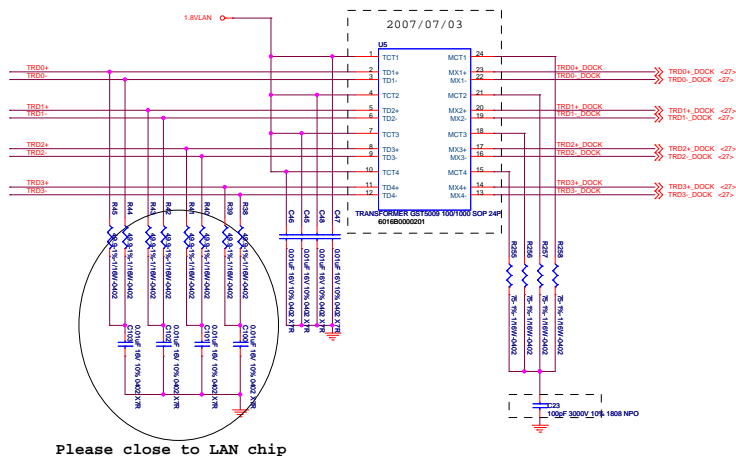
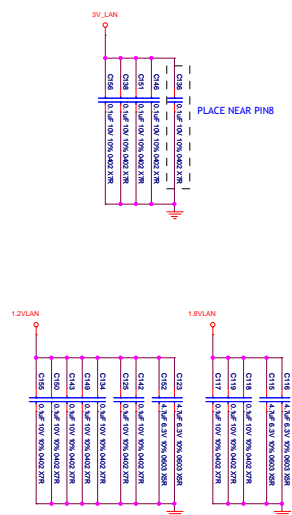
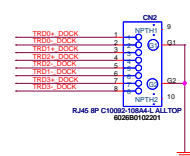
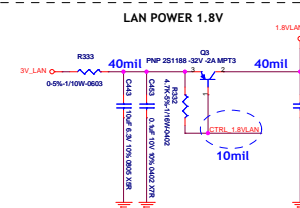
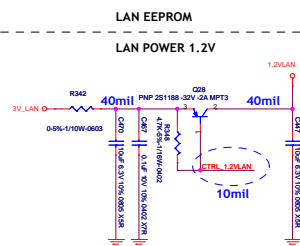
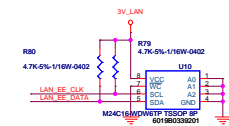
## PCIE Mini Card(WLAN)



## PCIE Mini Card for 3G



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Inventec Building, 66 Hou-Kang Street Shin-Lin District, Taipei 111, Taiwan TEL+886-2-2881-0721	
File	
Size	<b>M11D (Merom+Crestline+I</b>
Custom	<b>Mini Card/New Card</b>
Date	Wednesday, July 31, 2007
	Sheet 28



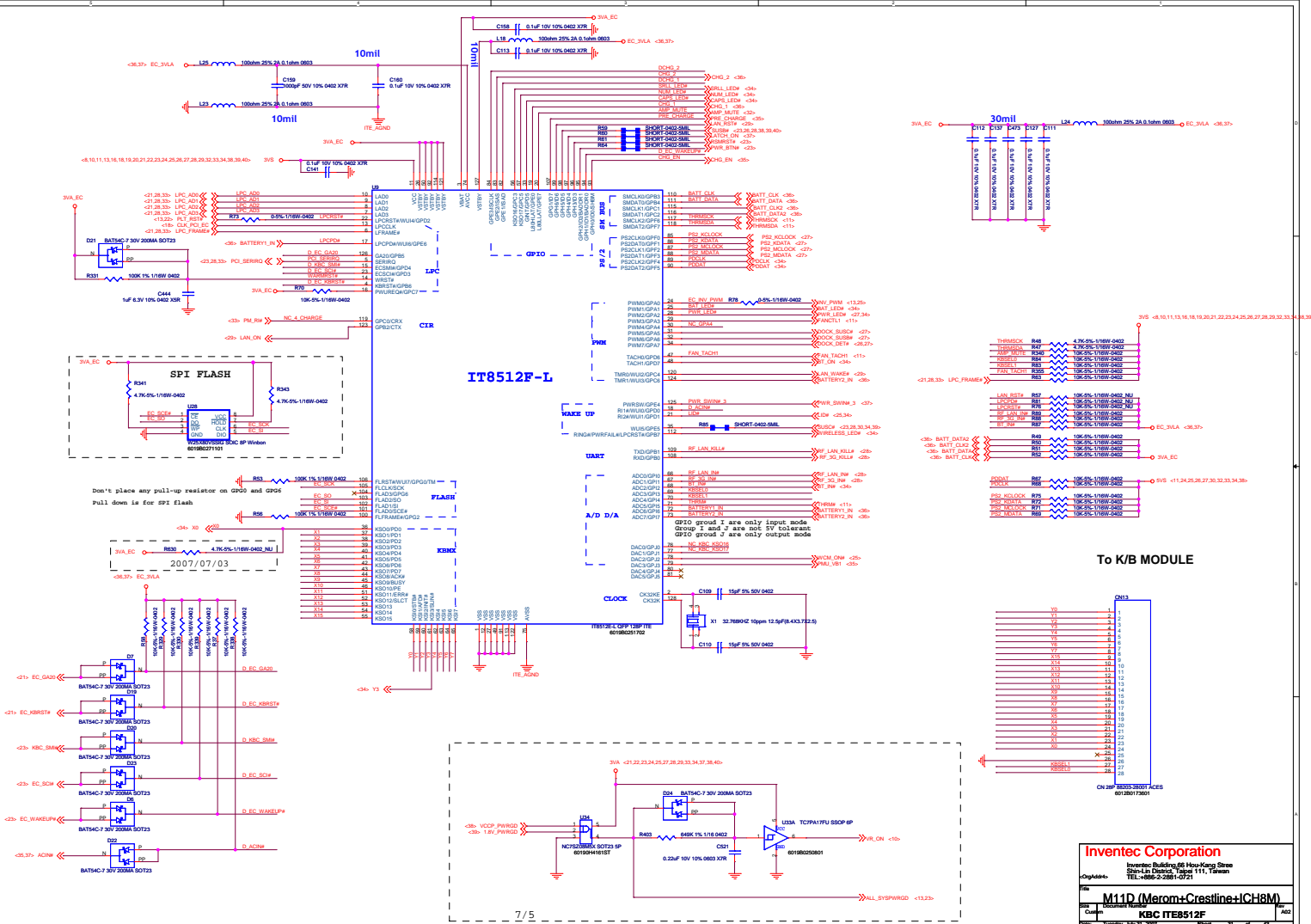
Please close to LAN chip

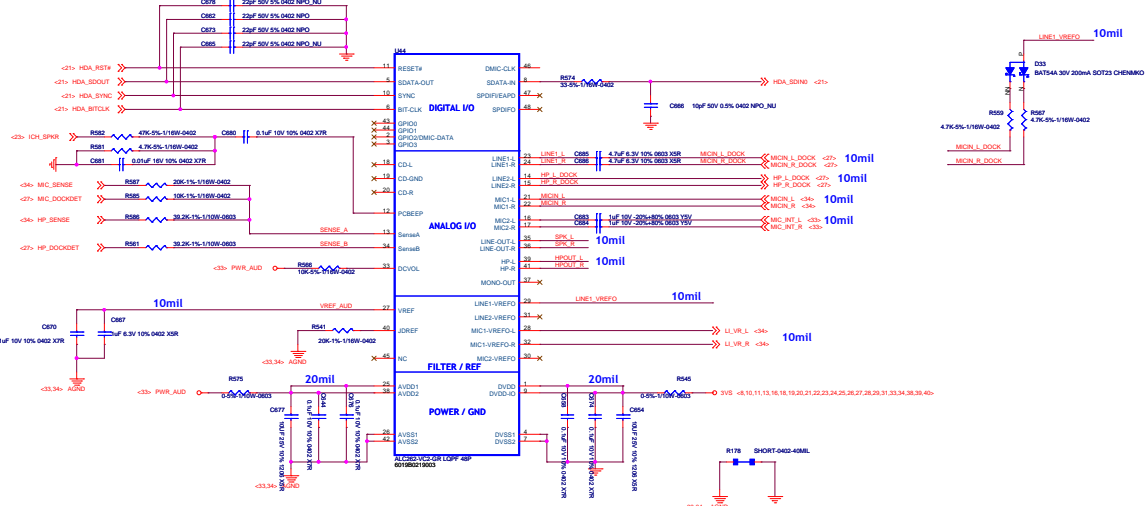
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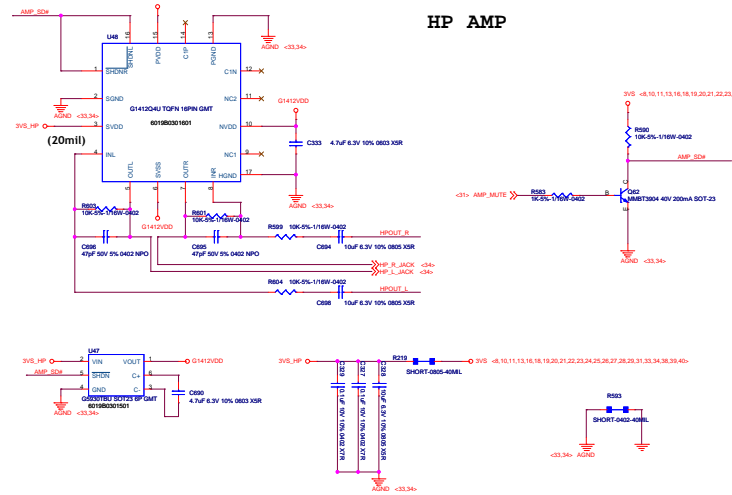
Title		<b>M11D (Merom+Crestline+ICH8M)</b>	
Size	Document Number	File	
<b>C</b>	<b>LAN (88E8055B0)</b>		
Date		Page	of
Tuesday, July 31 2007		29	43



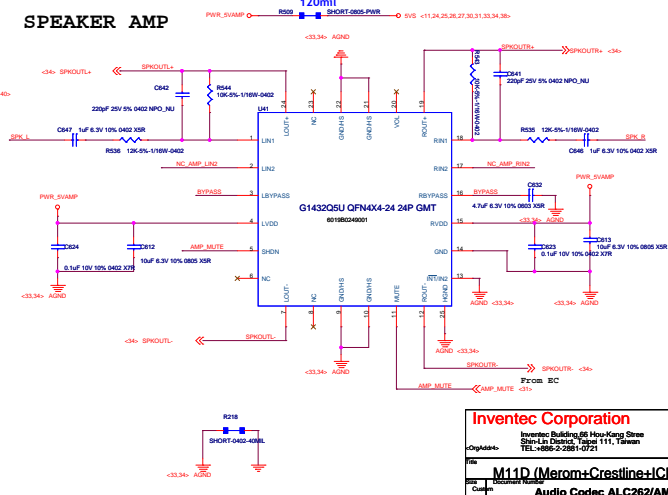




HP AMP



SPEAKER AMP



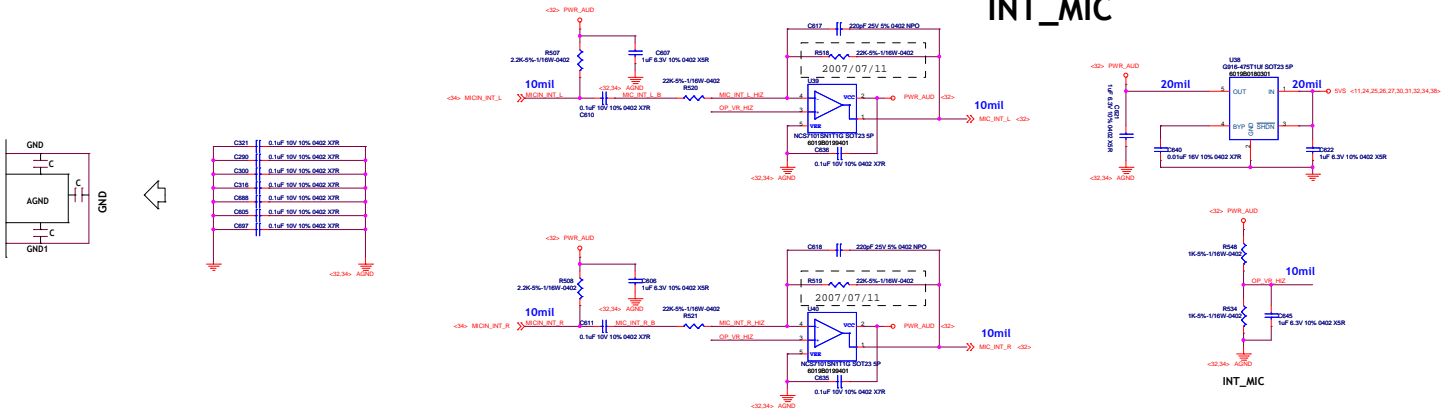
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Shih-Lin District, Taipei 111, Taiwan  
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**M11D (Merom+Crestline+ICH8M)**  
Audio Codec ALC262/AMP

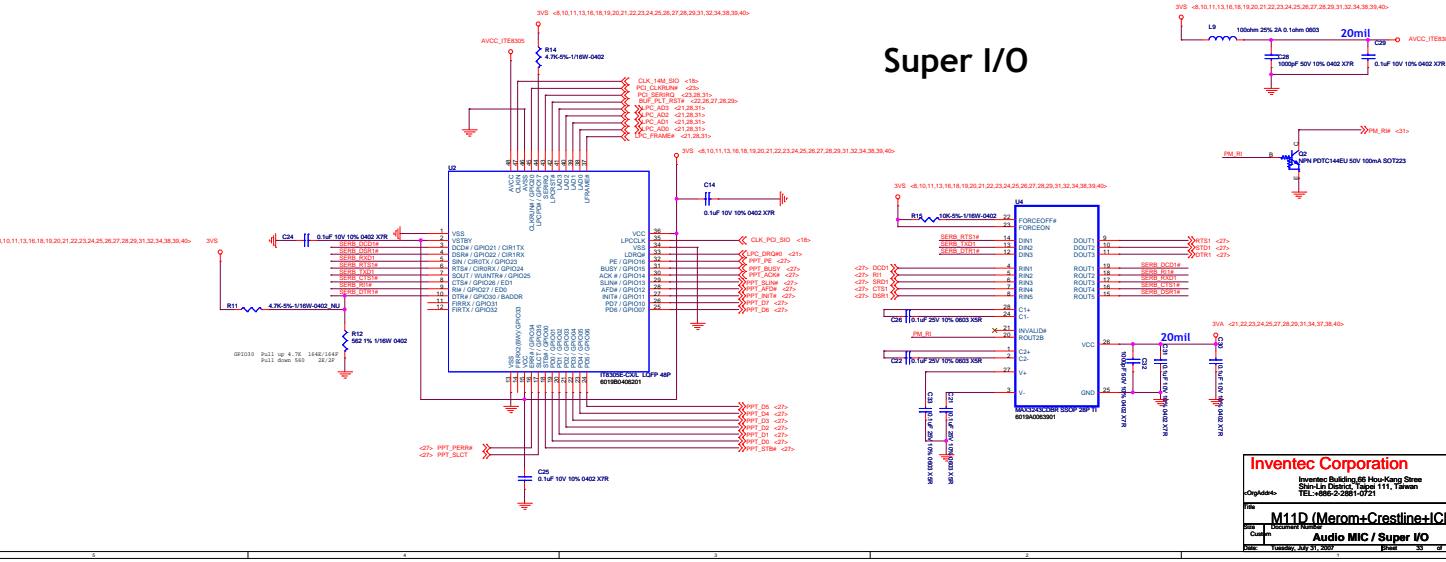
Rev: 1.00 Date: 08/08/08



INT\_MIC



Super I/O

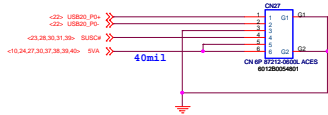


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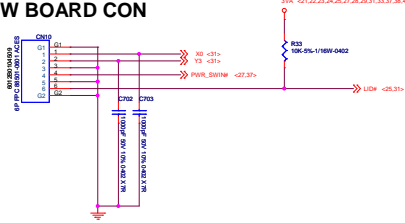
**M11D (Merom+Creline+CH8M)**  
Audio MIC / Super I/O

Rev: 1.00 Date: 2007.07.25

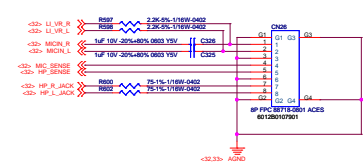
## USB Board CN



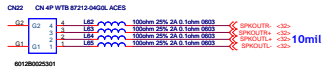
## SW BOARD CON



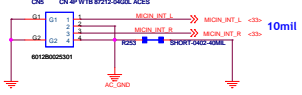
## Audio/B CN



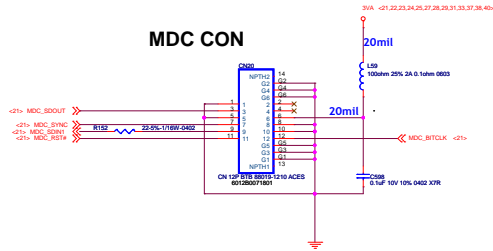
## INT\_SPK\_CN



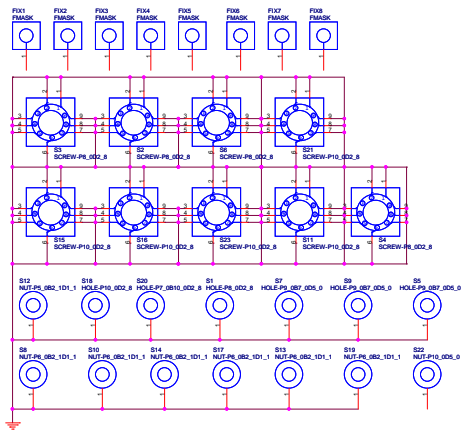
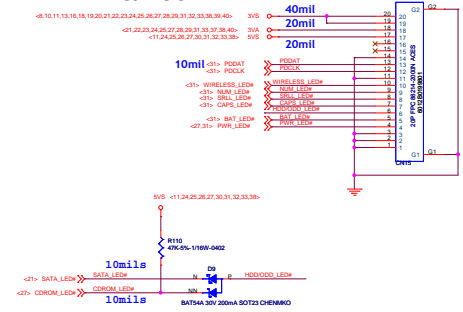
## INT\_MIC\_CN



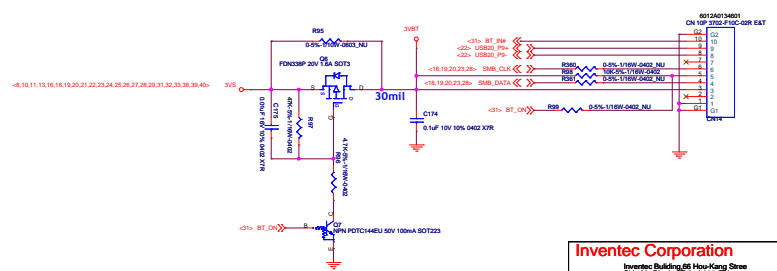
## MDC CON



## G/P CON



## Bluetooth CON.



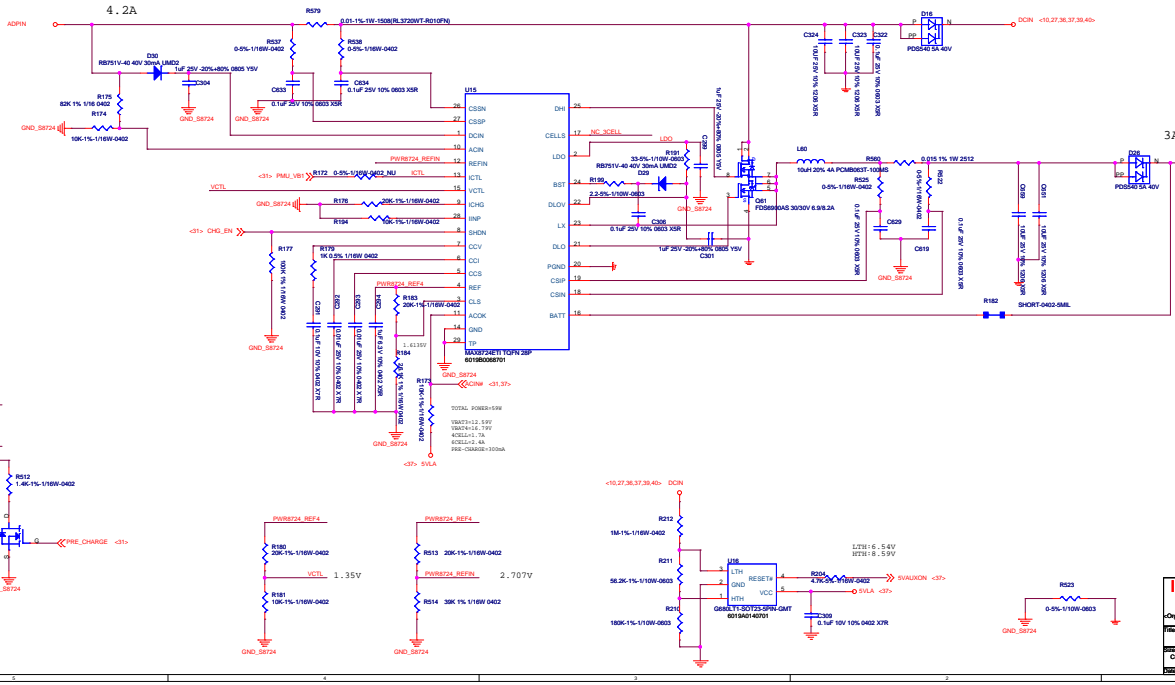
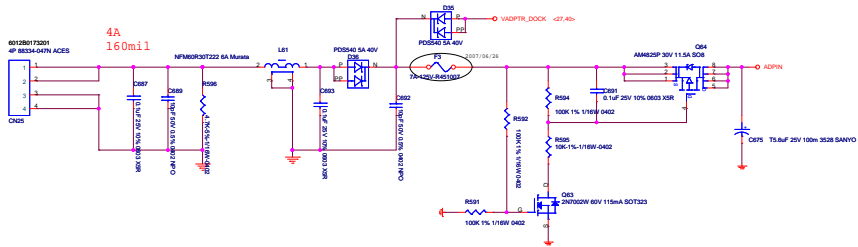
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M11D (Merom+Crestline+CH8M)

Board CN(MB Side)

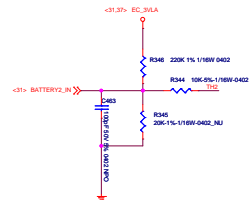
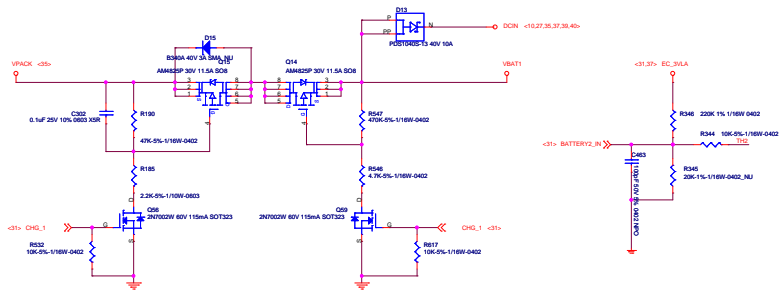
Rev: 1.00 Date: 07-2007



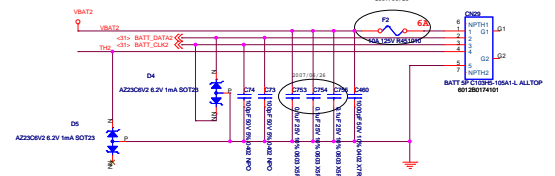
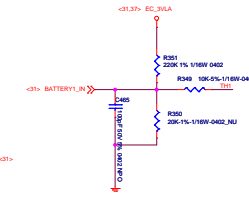
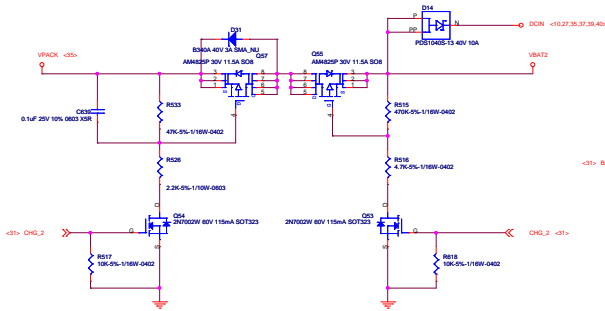
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**M11D (Merom+Crestline+CH8M)**  
Adaptor In/Charge

Rev: 1.00 Date: 2007-07-20

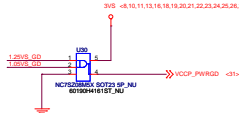
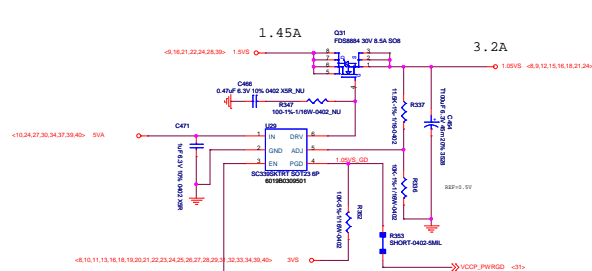
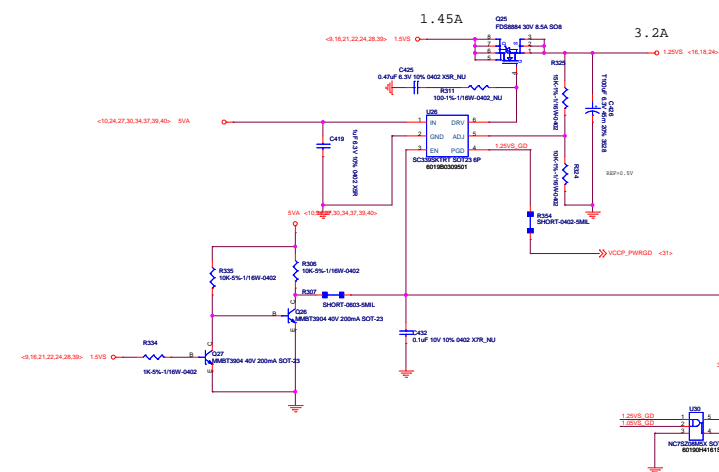
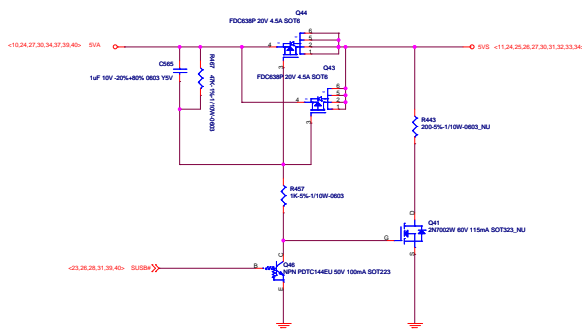
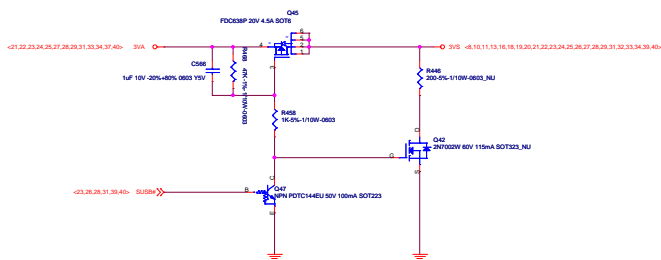


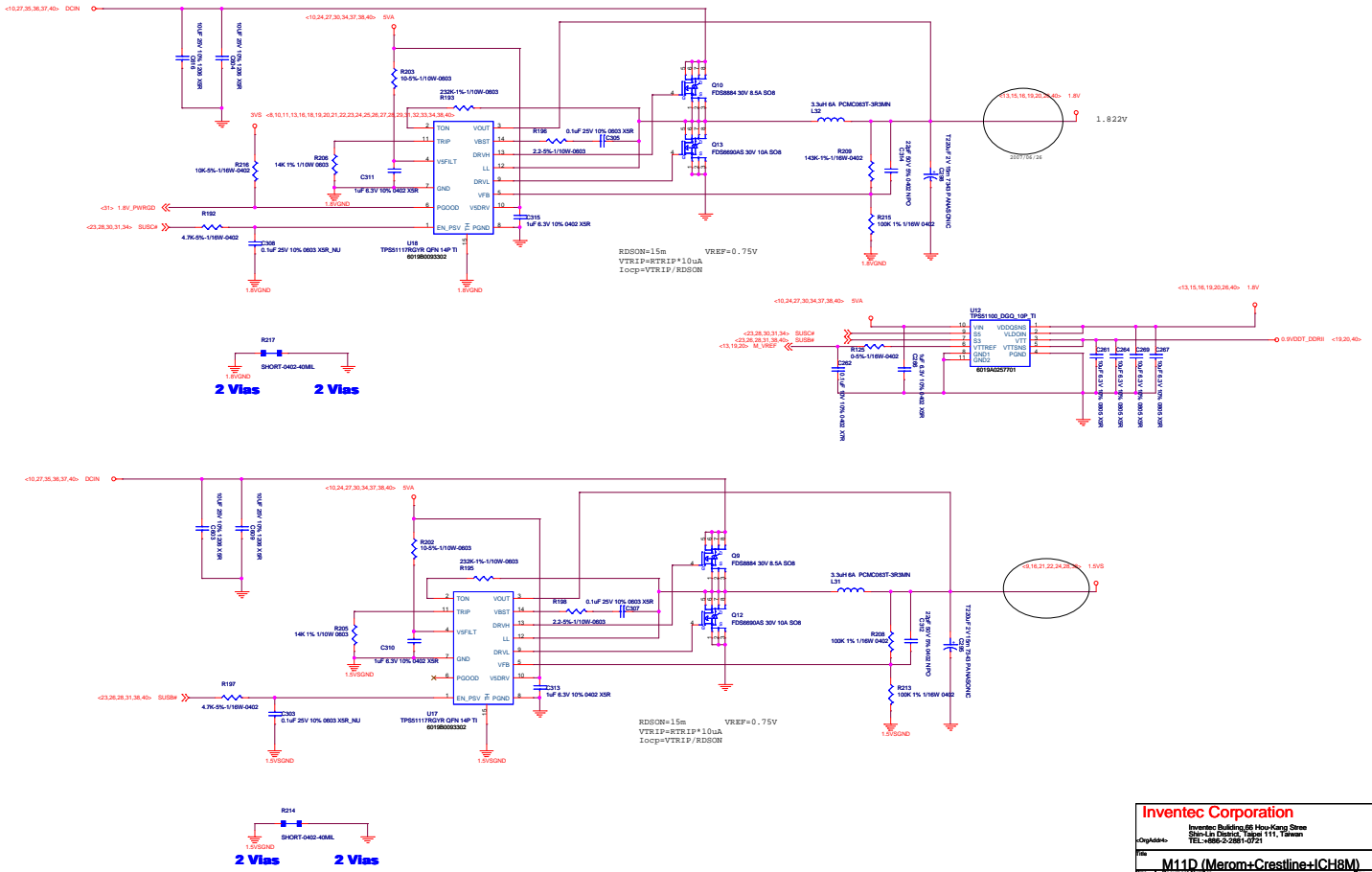
20mil



20mil







GFX\_CORE

<10,11,13,16,18,19,20,21,22,23,24,25,26,27,28,29,31,32,33,34,36,38>

<10,24,27,30,34,37,38,39>

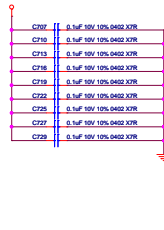
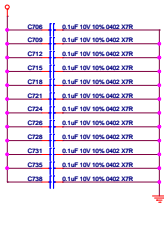
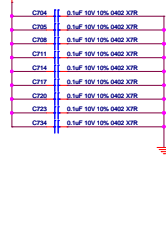
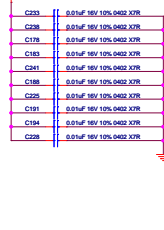
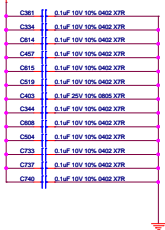
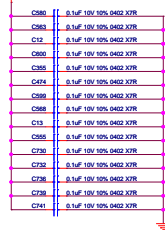
<19,20,38> 0.5V DOUT\_D08H

1.8V <10,16,18,19,20,26,38>

DCIN <10,27,36,38,37,39>

VAPTR\_DOCK <27,39>

3V5 <1,22,23,24,25,27,28,29,31,32,34,37,38>



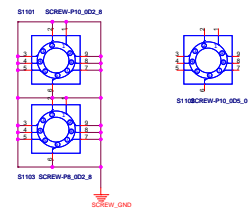
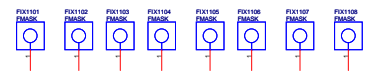
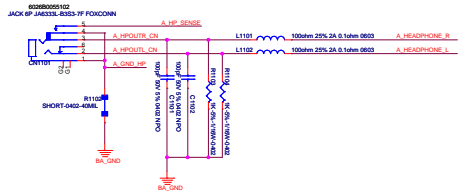
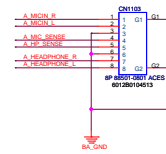
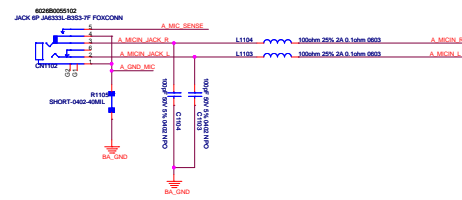
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Shih-Lin District, Taipei 111, Taiwan  
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**M11D (Merom+Crestline+CH8M)**  
**GPU Core**

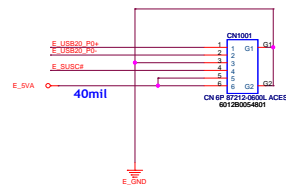
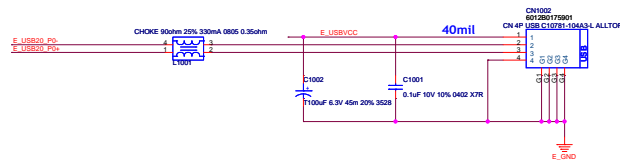
Rev: 1.00 Date: 2007.07.20



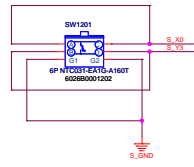
## AUDIO BOARD



# USB BOARD



## WIRELESS LAN BUTTON



## POWER SWITCH

